Demonstration and Performance Analysis for the Off-Ramp Portion of an All-Optical Access Node

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***Abstract*—Ultrafast processing of packets is demonstrated and the performance analyzed for the off-ramp portion of an all-optical access node. The off-ramp consists of synchronized fiber lasers driving an all-optical header processor that includes nonlinear optical loop mirrors (NOLM), electrooptic router, and demultiplexer in the form of a two-wavelength NOLM. We achieve switching contrasts of 10:1 for the header processor and demultiplexer with switching energies of 10 pJ and 1 pJ, respectively. Also, a proposed measurement technique to obtain eye diagrams is used to analyze the all-optical header processor using the synchronized lasers. Using this technique, we obtain an eye diagram with a Q value of 7.1 ± 0.36, which corresponds to a worst case BER value of 8.8×10^{-12} for a 95% confidence level. Finally, simulation models are used to verify and compare the experimental results, and we find good agreement. We also use the model to study the various causes for the degradation of the Q value through our system.**

***Index Terms*—Communication system performance, nonlinear optics, optical fiber communication, optical fiber switches, optical fiber systems, optical logic gates.**

I. Introduction

As single-channel speeds exceed electronic limitations for packet processing in time-division multiplexing (TDM) networks, all-optical packet processing becomes necessary to avoid speed bottlenecks. Toward this goal, we experimentally demonstrate the packet drop (off-ramp) functions for an all-optical access node for a 100 Gb/s packet network, and we analyze this performance using an eye diagram measurement technique to look at the statistical bit error rate (BER). By integrating synchronized fiber lasers [1], all-optical header processor in the form of nonlinear optical loop mirrors (NOLM) [2], electrooptical packet router, and payload demultiplexer, we demonstrate an integrated system as opposed to individual components. This also allows us to study the system performance of the all-optical off-ramp.

The integration gives insight into some of the key challenges of 100 Gb/s packet TDM networks, including multiple levels of all-optical logic gates operation, synchronization between the incoming data and the local source, and power budget for operation of the node. This demonstration shows the intercompatibility of the various optical components as well as the network functionality of the all-optical header processor and demultiplexer. Using an 8-bit, 100 Gb/s word, we achieve 10:1 contrast ratios from the header processor and the demultiplexer and 17 dB contrast ratio from the packet router.

Beyond demonstrating the functionalities, measurement techniques must be devised to test the error performance of these ultrafast devices. Currently, the method to measure the performance of a telecommunication device is to use a bit error rate (BER) tester, which sends a long bit pattern to the test device and counts the number of errors that occur through the device. However, these BER testers are currently limited to about 15 Gb/s. Therefore, to overcome this limitation, we use a method based on a sampling technique [3], using a cross-correlator and reference pulse. This allows the measurement of eye diagrams with picosecond resolutions. However, the speed of the technique is limited to the sampling speed. We apply this technique to the all-optical header processor and obtain an eye diagram with a Q value of 7.1 at 12 pJ switching energy for the header processor. This Q value corresponds to a statistical BER value of 7.0×10^{-13}.

There have been previous subsystem demonstrations using semiconductor devices and simplified architectures. Cotter *et al.* route 100 Gb/s, six bit packets using a single AND-gate as the header processor [4]. The use of a single AND-gate to process the header requires special bit patterns for the AND gate to be able to distinguish the headers. In addition, Glesk *et al.* demonstrate all-optical address recognition and self-routing in a 250 Gb/s packet-switched network [5], in which a switch operating on only one bit for each packet is used. Unlike these previous demonstrations, our node architecture enables more general optical serial processing capabilities because of increased flexibility through the possibility of using multiple levels of logic operations. The fiber-based NOLM's, which are used as the optical logic gates in this paper, have been shown to have unique properties such as ultrafast speed, cascadability, and Boolean completeness [2]. Although only two levels of logic operation have been demonstrated in this paper, further levels of operation are possible because the logic gates are regenerative. Multiple levels of logic operation permit multiple processing on the header, for example, to check empty packets, bit errors, or special conditions.

This article focuses on two aspects of the packet processing capabilities for the off-ramp. The first aspect, described in Sections II and III, is the functionality of the off-ramp with

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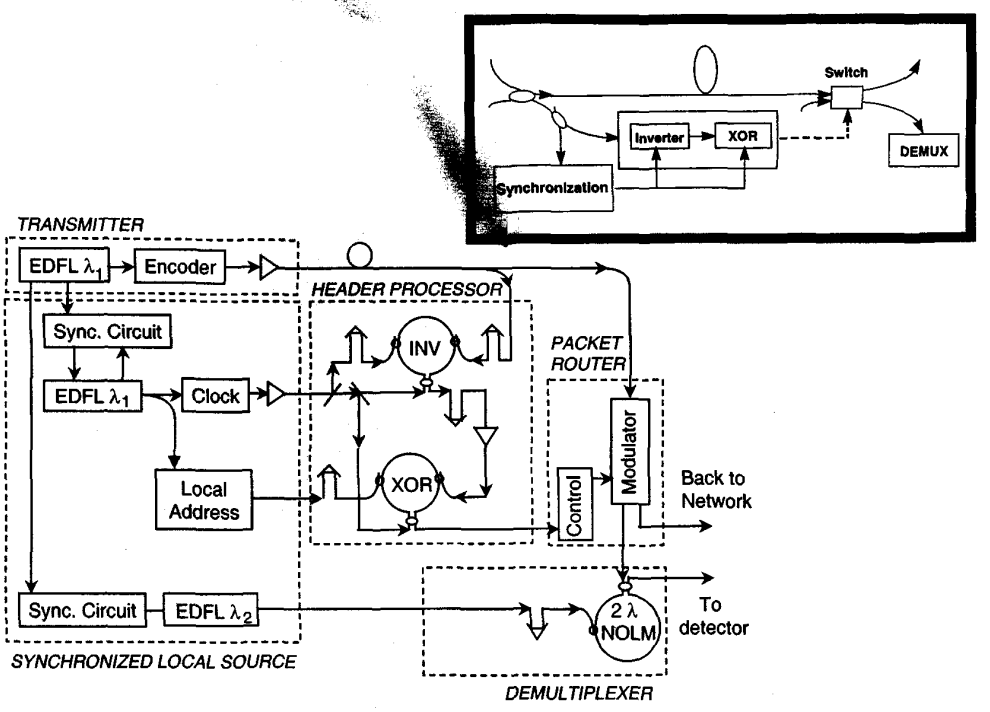

Fig. 1. Block diagram and detailed diagram for the off-ramp experiment. The transmitter consists of a master laser and a packet encoder. The off-ramp part consists of synchronized local lasers, a local header generator, a clock pulse train generator, a header processor, a packet router, and a demultiplexer. (INV = inverter, XOR = exclusive OR, 2λ NOLM = two-wavelength nonlinear optical loop mirror, and EDFL = erbium-doped fiber laser.)

focus on switching contrasts and switching energies. Then in Sections IV and V, the second aspect, system performance is discussed with the focus on potential statistical BER measurements of the off-ramp. To start with in Section II, we describe the experimental setup for the off-ramp portion of the access node. Then, in Section III, we present the experimental results for the packet processing. In Section IV, we describe the system performance measurement technique and the experimental setup for that measurement, and in Section V, the experimental results for the eye diagram are presented. Subsequently, in Section VI, we compare the experimental results with simulation models for analysis of our results and for discussion about future designs. Finally, we conclude with a summary of our results and discuss future work for the all-optical access node.

II. Experimental Setup for Access-Node

Fig. 1 shows a detailed experimental setup with a simplified block diagram for the off-ramp in the inset. The incoming packet from a distant transmitter enters the node. Upon entering the node, part of the packet energy is tapped to the header processor, and the rest is passed to the router through a delay line. In the node, a local laser, which is synchronized to the incoming packet rate, is used to generate the local clock pulses and the local address. The header processor, consisting of an inverter and an XOR gate, processes the incoming packets and controls the switch/router. A demultiplexer reads the payloads of the incoming packets using another synchronized local laser of a different wavelength.

The transmitter, which consists of a fiber laser (master laser) and an encoder, produces 8-bit packets (3-bit header "101," 5-bit payload "10010") that are sent to the node. The synchronized local laser (slave laser #1) with the same wavelength as the master laser passes through a clock encoder to generate clock bit patterns and a local address encoder to generate the local address pattern for the all-optical inverter and XOR gates. The inverter determines whether the incoming packet is empty or not. An empty packet would have header bits that are all "1." If the packet is not empty, then the inverter sends an inverted header pattern to the XOR gate. A local address generator sends the inverted local address to the XOR gate. If the header and local address match at the XOR gate, then there is no output, and the packet will go to the demultiplexing unit. If the headers do not match, the XOR gate output has at least one bit that is "1," which will trigger the control of the packet router to shift the packet back to the network. The payload in the packet goes to the demultiplexer, which is a two-wavelength nonlinear optical loop mirror (2-λ NOLM) driven by the other synchronized local laser (slave laser #2) with the wavelength different from that of the transmitter [1], [2].

The master laser and the slave lasers are passively mode locked, Er/Yb codoped fiber lasers [6]. The pulse widths are 2 ps at 1535 nm for the master laser and slave laser #1 and at 1543 nm for the slave laser #2. Synchronization of the master laser and the slave lasers is achieved by sending a separate clock pulse from the master laser to the slave lasers [7]. Although the laser repetition rate is 21 MHz, splitting each laser pulse and combining them with couplers and delay

lines to have pulse-to-pulse separations of 10 ps creates 100 Gb/s words. The local laser pulse is aligned to the first pulse of the packet. Therefore, the clock and local header align to the header and payload automatically for fixed header and payload lengths.

This synchronization is designed to force the local lasers to follow the slow drifts of the remote clock pulse rate and to simulate an all-optical clock recovery in the network. The response bandwidth of the synchronization circuit is 10 kHz and it is limited by the acoustooptic modulator (AOM). In addition, the speed of the circuit is limited by the optoelectronic detectors and the RF components used in the phase locked loop circuit design. In this experiment, we use 1 GHz RF components and the synchronization is limited by the maximum frame rate of 1 GHz. However, in a real network design, an access node should recover both timing of packet and bit separation. With this synchronization scheme this would be possible for low repetition rate applications because of the limitations of electronics at high frequencies.

The all-optical logic gates are constructed by using low birefringent nonlinear optical loop mirrors (low-bi NOLM's). The low birefringence ($\Delta n \sim 10^{-6}$) is obtained by wrapping fibers with very low background birefringence on aluminum mandrels. This technique allows for longer interaction lengths between copropagating, orthogonally polarized pulses than in conventional polarization maintaining fiber while maintaining a high polarization extinction ratio (PER$\sim$40 : 1). An advantage of this kind of optical logic gate is its cascadability. Because the logic gate is also regenerative, this allows multiple levels of all-optical logic operation. Another advantage is the timing window, which makes the NOLM's tolerant to possible timing jitter between the bits. The logic gates have switching energies of 10 pJ/pulse, timing windows of 5 ps, and nonlinear transmissions of 50% [2].

The demultiplexing and packet routing use guided-wave optical structures. The 2-λ NOLM with a timing window of 6 ps demultiplexes the payload into individual bits. This 2-λ NOLM uses a high nonlinearity, dispersion-shifted fiber ($\lambda_0 = 1530$ nm), which has a smaller core size (effective area $A_{\text{eff}} = 17\ \mu\text{m}^2$) to increase optical intensity and a higher germanium doping to increase the intrinsic nonlinear coefficient. The effective nonlinearity is 4.4 times that of a normal dispersion-shifted fiber. The switching energy of this device is less than 1 pJ/pulse. A commercial 2×2 $LiNbO_3$ modulator is used as the packet router.

III. Experimental Results for Access Node

The output of the various components of the all-optical off-ramp is measured by using a cross-correlator. Because the pulses are only 10 ps apart in our packets and because we are looking at energy contrasts of the individual pulses, the cross-correlator gives us the most relevant information. We use a fixed reference pulse as one of the inputs to the cross-correlator.

The output for the header processor is shown in Fig. 2. Fig. 2(a) shows the incoming data packet, including the header bits, "101." The inverted header output, "010," from the

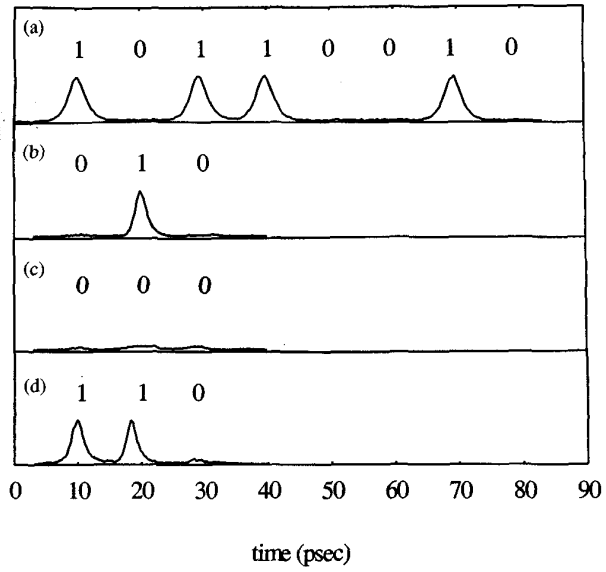

Fig. 2. Cross-correlation results for the header processor. (a) Input data packet. (b) Output of the inverter. (c) Output at the XOR gate when the headers match. (d) Output at the XOR gate when the headers do not match (the inverted incoming header is 010 and the local header is 100).

inverter is shown in Fig. 2(b) with an intensity contrast of $\geq$10 : 1 between the "1" and "0." This output is used as the input to the XOR gate. Figs. 2(c) and (d) shows the XOR gate output when the header and the local address match and not match, respectively. In both cases, the intensity contrast between the "1" and "0" is at least 10 : 1. This contrast ratio is limited by the in complete switching caused by pulse distortion due to nonsoliton pulse propagation and the induced chirp during the amplification of the pulses at the erbium-doped fiber amplifiers (EDFA's).

The output from the header processor containing the information of matched or unmatched header is used to drive the packet router with the results shown in Fig. 3. The packet router is a $LiNbO_3$ modulator. When the incoming header does not match the local address, the packet is routed back onto the network. The energy contrast ratio of the signal returning to the network over the leakage through the modulator is 17 dB. In this experiment, the performance of the demultiplexer is not affected by the packet router. However, when adding a new packet into the network, ON–OFF ratio of the router will be important. Theoretically, the ON–OFF ratio of 17 dB might cause a maximum amplitude modulation of ($\pm$)2.5% in packet addition due to the interference between the leakage and the new packet. A two-stage packet router can be used to prevent the interference problems.

When there is a match between the header and the local address, the packet is routed to the demultiplexer. The demultiplexed output for each channel is shown in Fig. 4. For channels (1–5), the pump pulse for the demultiplexer is delayed by 10 ps each time to select the appropriate bit. The contrast ratio is 10:1 between the "1" and "0" bits. Residual signals in the "0" bits indicate pump leakage and energy tails from the adjacent "1" bit of the payload. These residual signals are

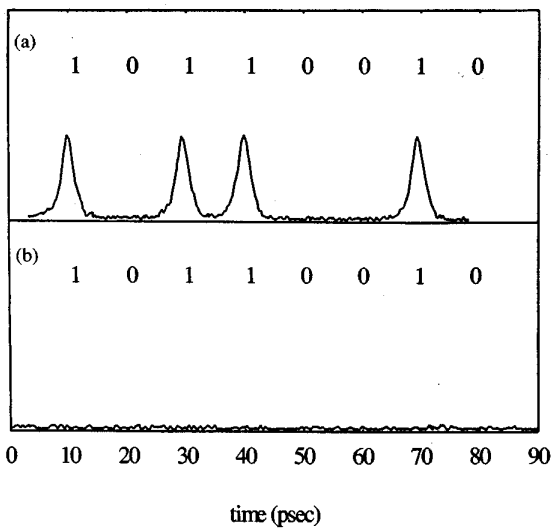

Fig. 3. Cross-correlation results of the output of the packet router. (a) The incoming header does not match the local header (packet sent back to network). (b) The header matches the local header (packet sent to demultiplexer).

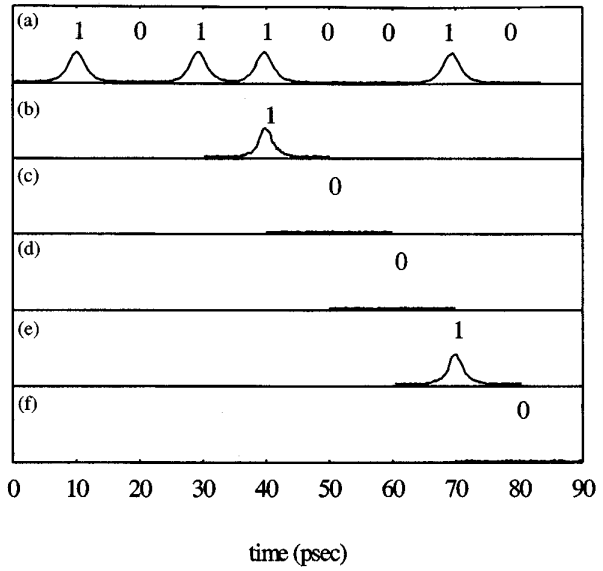

Fig. 4. Autocorrelation results of the demultiplexer. (a) Input data packet. (b)–(f) Output of the 2λ NOLM by adjusting the delay of the local pulse by an additional 10 ps each time.

not visible in Fig. 4 because we use an autocorrelation to see each individual bit, and the 10 : 1 contrast ratio is too high to distinguish the relative difference between "1"'s and "0"'s in the autocorrelation.

These preliminary results show intercompatibility of the all-optical components toward a packet TDM access node. The major challenges are multiple levels of all-optical logic operation, low jitter synchronization, and power budget. Our results prove that the fiber-based optical logic gates are cascadable and can be used to perform multiple levels of all-optical logic operation. The synchronization scheme used in this paper shows a very low timing jitter (<1 ps). By using low birefringence to increase the walk-off distance in the header processor, we have been able to lower the switching energy to about 10 pJ/pulse. The range of switching energies for the header processor is 5–15 pJ/pulse, and that for the demultiplexer is 0.5–1.0 pJ/pulse. The output switching contrast is directly related to the switching energy. However, if the input switching energy is too high, pulse distortion occurs in the loop mirror and the switching contrast will degrade. Here, the header is fixed to specify the destination address within the ring network structure. In order to have broadcasting capabilities, a special address can be added to the header and one more level of optical logic operation may be needed. To avoid errors from possible node failure, the packet router switch will be set to direct the data back to network when there is no power to the node.

IV. Eye-Diagram Measurement Technique and Experimental Setup

A sampling method to measure the eye diagram is applied to the header processor portion of the off-ramp using the synchronized fiber lasers. Using a cross-correlator with a reference pulse, we can measure the eye diagram with picosecond resolution for 100 Gb/s packets. The conventional bit-error-rate tester (BERT) does not have the required resolution to measure the eye diagram for such tightly spaced bits.

Fig. 5 shows the detailed experimental setup, and the inset shows the general overview for the setup. As in the previous setup, the synchronized sources for the header processor are the master laser, representing a transmitter and the slave laser, acting as the local laser. Both lasers produce 2 ps pulses at 1535 nm with a repetition rate of 21.6 MHz. Unlike the previous case, the encoder for the master laser now produces the packet pattern "0001011100" with 10 ps bit-to-bit separations. The reason for this particular pattern is that by taking some particular 3-consecutive bits of this pattern, we can form all of the possible 3-bit patterns that start with a "1" bit. This is important for looking at any pattern dependent effects on the performance of the header processor. The starting bit of the header packet must be a "1" for synchronization purposes and for feedback purposes in order to stabilize the system. Also, for this first bit, the first gate does not act as an inverter, which makes a "1" output at the first bit position for all of the four different patterns. The output from the slave laser passes through the clock encoder to produce the 3-bit pattern "111." As before, the inverter determines if the incoming packet is empty, and the XOR gate determines if there is a match to the local address.

We also use a feedback loop within the experimental setup to control timing drifts between the two gates caused by thermal expansion of the fiber in the first logic gate. A schematic of this feedback scheme is shown in Fig. 6. By using the fact that in our architecture, all of the header packets will start with a "1" bit for clock recovery purposes, we use this first bit for timing corrections within the header processor. Since the thermal change is slow, the feedback circuit can also be slow with the feedback loop checking roughly every 5 s. The feedback uses a cross-correlator (cross-correlator 2

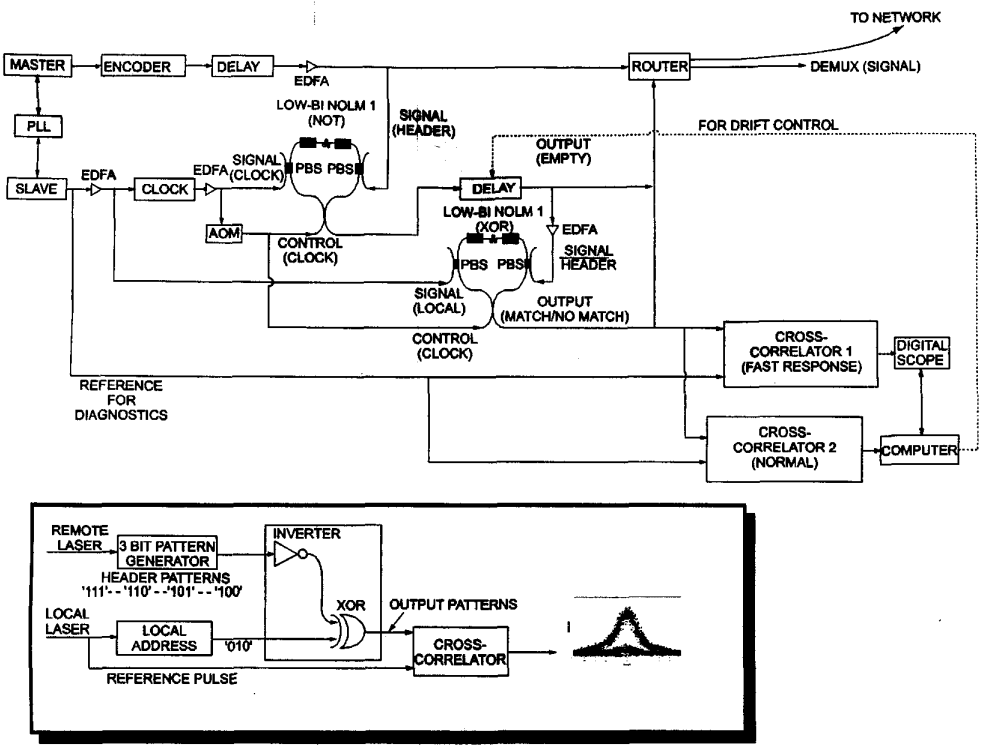

Fig. 5. Experimental setup for eye diagram measurement. The Master laser passes through the encoder producing "0001011100," and the Slave laser passes through clock producing "111." The output of the header processor, consisting of two NOLM's, is sent to cross-correlator 1 for measuring the eye diagram. Cross-correlator 2 is used for the feedback control. The solid lines are optical paths, and the dashed lines are electrical paths. (PLL = phase locked loop, NOLM = nonlinear optical loop mirror, AOM = acoustooptic modulator, EDFA = erbium-doped fiber amplifier, PBS = polarization beam splitter.)

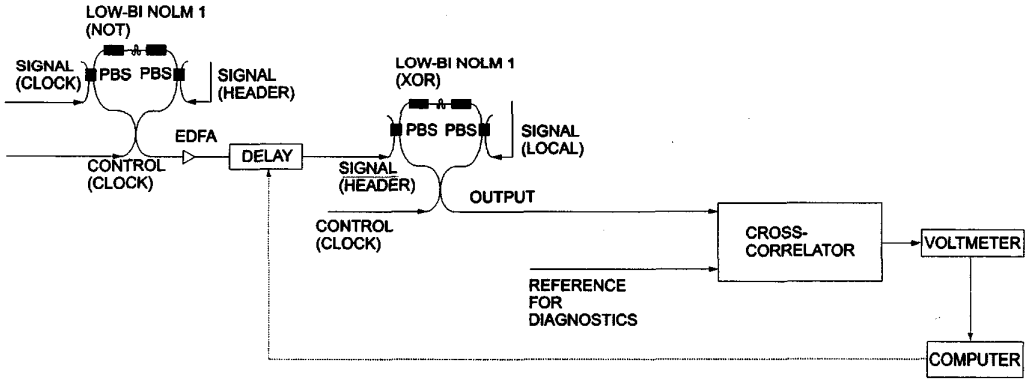

Fig. 6. Schematic of feedback loop for timing drift control. The first output bit of header processor is sent to a cross-correlator. Using the signal as feedback signal, the computer receives the signal from the voltmeter and controls the optical delay stage between the two logic gates. The solid lines are optical paths, and the dashed lines are electrical paths. (NOLM = nonlinear optical loop mirror, EDFA = erbium-doped fiber amplifier, PBS = polarization beam splitter.)

in Fig. 5) and an optical delay stage to maintain the timing between the cascaded gates. We set the gates appropriately so that the first bit, which is always a "1" bit, of the incoming header packet will produce a "1" bit in both gates. Then, by looking at the peak of the first bit output of the header processor with the cross-correlator and maximizing this value, we control the delay stage to maintain the timing between the two gates. This method works because the first bit is a constant value and because the timing drift due to thermal effects is slow, requiring only a slow adjustment. Without this feedback control, the timing would cause a degradation of switching contrast, which would degrade the performance.

The output of the header processor, which can be any one of four possible 2-bit patterns, is split and sent to the diagnostics for performance analysis. Cross-correlator 1 is carefully set up to use the fast response (~10 ns rise and decay time, packet separation of ~47 ns) of the photomultiplier tube (PMT) to remove any of the averaging effects. By using a digital scope to take single-shot scans of the signal from the PMT, a single pulse response is taken per scan. We take a

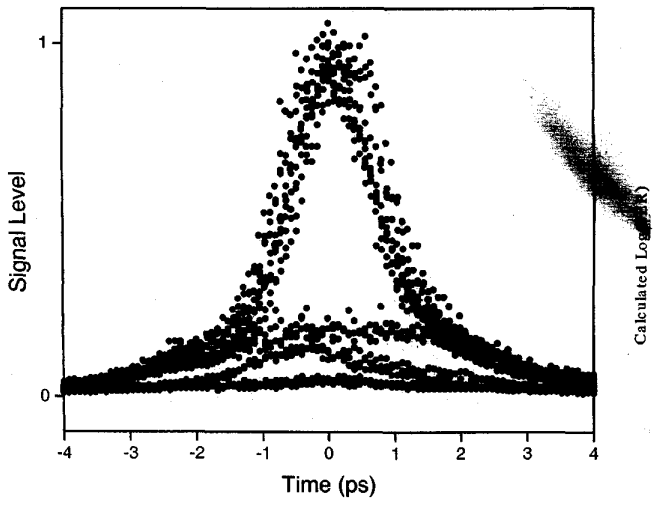

Fig. 7. Eye diagram of header processor (cross-correlation). This is the trace of the eye diagrams taken with the setup of Fig. 5 where the trace is taken by moving an optical delay stage in the cross-correlator. It is an overlay of all the different possible combinations of the 3-bit incoming header and the two possible values of "0" or "1" for the local bit.

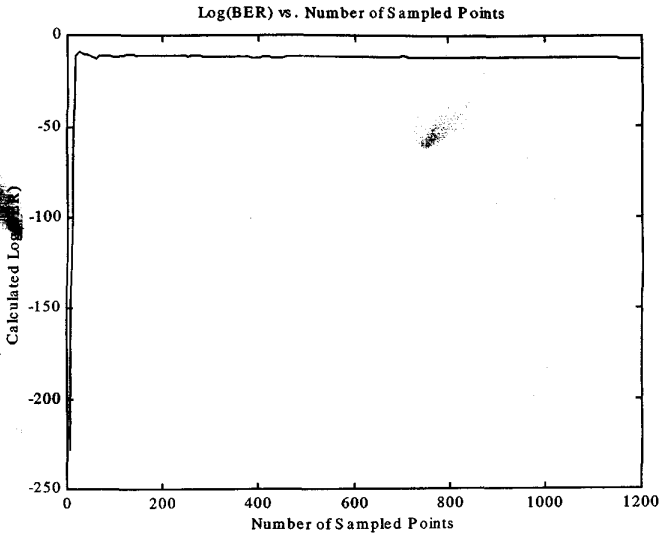

Fig. 8. Calculated Log(BER) versus number of data points. This shows that the performance of the header processor converges to a stable value after roughly 100 data points. By using 300 data points, the performance does not change, but only the error bar of the measurement is decreased.

large number of scans while varying the timing between the reference pulse and the output of the header processor. Then, by overlaying the scans, we can map out the eye diagram with picosecond resolution for all the possible patterns. There are a few limitations in this sampling technique, which will be addressed in the discussion section.

V. Performance Measurement Results and Analysis

The eye diagram for the header processor is shown in Fig. 7. This is one of several measurements that we have taken for the eye diagram. The eye diagram is for return-to-zero (RZ), hyperbolic secant pulses, and it is an overlay of all possible outputs from the header processor. The input headers are four nonrandom, but different and equal numbers of 2-bit patterns, and the local address bit may be a "1" or "0." Because there can be incomplete balancing for the NOLM when acting as an inverter or XOR gate, the "0" level will not be a true "0." This causes a finite switching contrast. Also, the NOLM has a finite polarization extinction ratio causing pump leakage to be present for both the "1" and "0" outputs. For the "1" output, the pump leakage is always present, which effectively adds a constant background. However, for the "0" output, there are two possible cases in the XOR ($\oplus$) gate. The "0" level can arise for the case without any pump pulses (i.e., $0 \oplus 0 = 0 +$ no leakage) and for the case with two-pump pulses (i.e., $1 \oplus 1 = 0 +$ leakage from two pump pulses + incomplete balancing). This leads to a spread of the "0" level in the eye diagram, where half of the "0"'s will be without any pump leakage and the other half with pump leakage and energy from incomplete balance within the NOLM. However, there is no such spread for the "1" level because the "1" output occurs when the NOLM is unbalanced and the leakage is always present. This leads to less distribution at the eye diagram as compare to the "0" output case.

By looking at the center points of the eye diagram as done by Matsumoto *et al.* [8], we can measure the Q parameter from which we can statistically calculate the potential BER. Unlike Matsumoto, who looks at the tail of the pulse, we look at the center of the eye for the "0" level because we must also consider the pump leakage, which will give the worst case. The Q parameter, which describes the quality of the received signal, is defined as

$$Q = \frac{I_1 - I_0}{\sigma_1 + \sigma_0} \tag{1}$$

with I_1 and I_0 being the sampled means of the "ON" and "OFF," respectively and with σ_1 and σ_0 being the sampled standard deviations of the "ON" and "OFF," respectively [9]. The statistical BER is given by

$$\text{BER} = \frac{1}{2}\,\text{erfc}\left(\frac{Q}{\sqrt{2}}\right) \tag{2}$$

where the *erfc* is the complementary error function based on the assumption of Gaussian distribution. For each 2-bit pattern, 300 data points are taken. Because there are four different possible 2-bit patterns, the total number of data points is 1200. In addition, because the local bit can be "0" or "1," there are 1200 data points for the "1" level and the "0" level. With these points, we find a Q value of 7.1 for the eye diagram of Fig. 7, which corresponds to a BER of 7.0×10^{-13}. We measured the Q value 5 times with the measured values all within 10 percent of each other, thus showing a repeatability of the measurement.

As a check, we look at the Q value versus the number of data points to make sure that the 300 data points per pattern is valid. Fig. 8 shows the calculated Log(BER) versus the number of sampled points corresponding to the data of Fig. 7, and we can see that the performance result converges fairly rapidly and stays relatively constant after the first 100

overall points. Therefore, we can see that taking more points per pattern only reduces the error bar of the measurement without changing the end result.

Because this is a statistical method, we must look at the associated confidence interval to calculate possible errors in the measurement. The confidence interval is an interval of values that contains the true value of a parameter with a given confidence level. For a given system, the confidence interval for the mean [10] is given by

$$P\left[I_n - t_{n-1,1-\alpha/2}\frac{\sigma_n}{\sqrt{n}} < \mu < I_n + t_{n-1,1-\alpha/2}\frac{\sigma_n}{\sqrt{n}}\right] = 1-\alpha \quad (3)$$

and the confidence interval for the variance is given by

$$P\left[\frac{(n-1)\sigma_n^2}{\chi^2_{n-1,1-\alpha/2}} < \sigma^2 < \frac{(n-1)\sigma_n^2}{\chi^2_{n-1,\alpha/2}}\right] = 1-\alpha \quad (4)$$

where I_n is the sampled mean, μ is the (unknown) true mean, σ_n is the sampled standard deviation, σ is the (unknown) true standard deviation, n is the number of sampled points, and $(1-\alpha) \times 100\%$ is the confidence interval level. The $t_{v,p}$ and the $\chi_{v,p}$ are the standard t-distribution and the chi-square distribution, respectively, with subscripts being appropriately substituted with the subscripts defined by the confidence intervals. By looking at the confidence interval and setting the confidence level to 95%, we can calculate the error range of the Q value to be from 6.7 to 7.4 for the eye diagram of Fig. 7. This means a worst case BER of 8.8×10^{-12} and a best case BER of 4.8×10^{-14}. Note that this error range is inversely related to the number of sample points for a given confidence level. While this method has a better resolution than the regular BERT, the BERT typically uses many more data points. Therefore, the confidence level for a BERT result can be much higher than this sampling technique.

To test the variation in parameters of this technique, we also look at the performance of the header processor as a function of input packet pulse energy. To study this, we measure the Q value of the header processor while varying the pulse energies of the incoming packet. We start with an input pulse energy of 12 pJ and decrease it at increments of 2 pJ for a total of four sets.

Fig. 9 shows the variation of (a) the Q value and (b) the extrapolated BER value as the input packet pulse energy is varied. The error bars on the data points are calculated with a 95% confidence interval level, and the range of the error bars is defined by the confidence interval. Because the ratio of error range over the measured value is nearly constant for a given confidence level, the error bars are larger for the higher Q values (lower BER). We find that both the Q values and the corresponding BER values degrade linearly with the input power. This is primarily caused by the degradation of the switching contrast of the gates, which also degrades linearly with the switching energy.

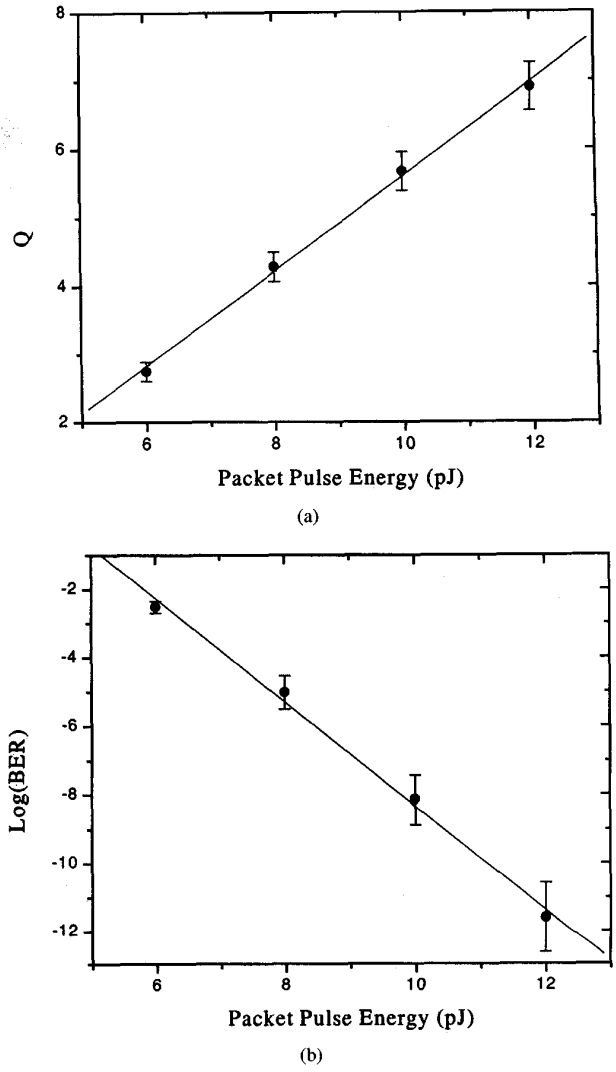

Fig. 9. Results for various incoming packet pulse energies. Looking at the center of the eye diagram, we measure (a) the Q value and (b) the calculated BER while changing the pulse energy of the incoming packet. Error bars are set for 95% confidence level.

VI. Modeling and Simulation Results

We also compare our experimental results with results of a simulation that we developed. In our simulation, we try to separate each parameter, which can degrade the Q value. For the header processor, there are several sources of noise that we must take into account. These include the laser sources, amplifiers, timing jitter, and intersymbol interference (ISI). In addition, the incomplete switching/balancing of the NOLM's along with the pump leakage can enhance these noise effects. Because it is not possible in the experiment to separate out each of these sources of noise, we look at a simulation model to understand the significance for each cause of noise.

Before we look at the full model, we look at the noise parameters for our system. The source is a passively mode-locked fiber laser where the noise of concern is the amplitude fluctuation in the pulses. We measure the amplitude jitter by looking at the fundamental harmonic of the repetition rate [11], and we find the variance of the amplitude fluctuation to be 6.67 for the master laser and 3.37 for the slave laser. With

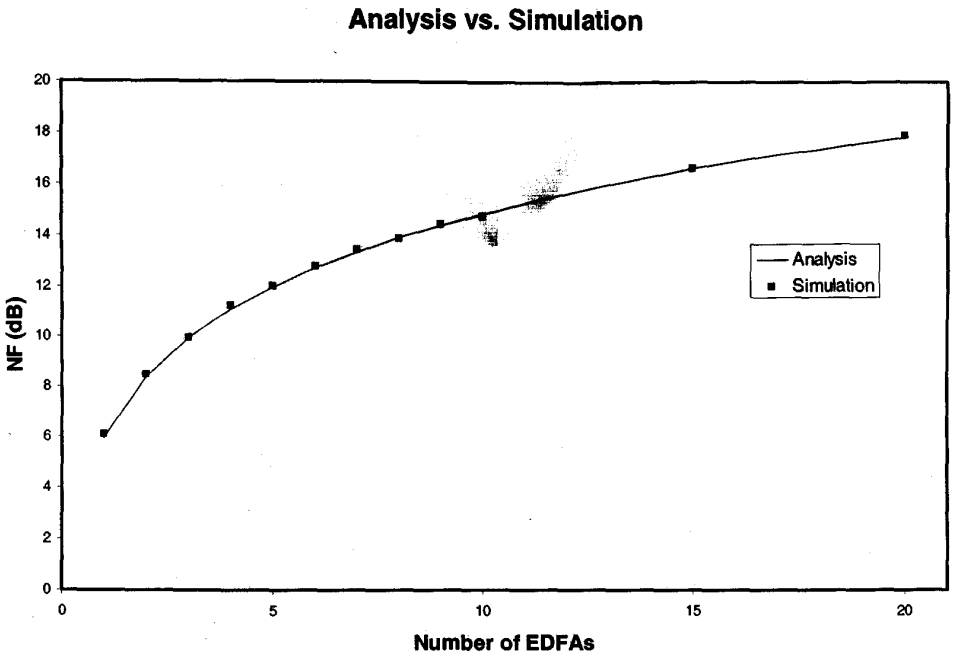

Fig. 10. Test of numerical EDFA model versus analytical EDFA model for cascaded amplifiers. The NF is calculated for various numbers of cascaded amplifiers.

this measurement, the input SNR is 36.6 dB for the incoming packets and 43.4 dB for the locally generated clock signals. For the amplifiers, which are EDFA's, we base our model upon the work of Desurvire [12]. In the EDFA model, the gain is given by

$$\langle n(z)\rangle = G(z)\langle n(0)\rangle + N(z) \tag{5}$$

where $n(z)$ is the output number of photons that is directly proportional to the output power, $n(0)$ is the input number of photons, and $G(z)$ is the overall gain of the amplifier. $N(z)$ is given by

$$N(z) = \frac{\eta N_2}{\eta N_2 - N_1}(G-1) = n_{\rm sp}(G-1) \tag{6}$$

where N_2 and N_1 are the populations of the upper and lower energy levels, respectively, η is the quantum efficiency of the amplifier, G is the gain, and $n_{\rm sp}$ is the spontaneous emission factor. The variance of this output signal is given by

$$\sigma^2(z) = \langle n^2(z)\rangle - [\langle n(z)\rangle]^2 \tag{7}$$

and substituting in (5), we obtain

$$\sigma^2(z) = G^2(z)\lfloor\sigma^2(0) - \langle n(0)\rangle\rfloor + G(z)\langle n(0)\rangle + N(z) + 2G(z)N(z)\langle n(0)\rangle + N^2(z) \tag{8}$$

where $\sigma(0)$ is the standard deviation of the input signal. We also look at the noise figure (NF) of the amplifiers, which is given by

$$\text{NF} = \log(\text{SNR}_i) - \log(\text{SNR}_o) \tag{9}$$

where SNR_i is the signal-to-noise ratio of the input signal to the amplifier and SNR_o is the signal-to-noise ratio of the output signal from the amplifier. The SNR is represented by

$$\text{SNR}_i = \frac{\langle n(0)\rangle^2}{\sigma^2(0)}$$
$$\text{SNR}_o = \frac{\langle n(z)\rangle^2}{\sigma^2(z)}. \tag{10}$$

Substituting in the above equations, we find the general expression for the NF to be

$$\text{NF} = \frac{\text{SNR}_i}{\langle n(0)\rangle}\left\{\frac{\sigma^2(0)}{\langle n(0)\rangle} - 1 + \frac{1+2N(z)}{G(z)} + \frac{N(z)[N(z)+1]}{G^2(z)\langle n(0)\rangle}\right\} \tag{11}$$

where by using the experimentally measured values of $n_{\rm sp}$ and $G(z)$, we can calculate $N(z)$ and then solve for $\sigma^2(z)$ and NF. Because this is the general expression for NF, the NF depends upon the input mean and variance. We can experimentally measure the $n_{\rm sp}$ for the amplifiers using the standard method [13] with the formula

$$NF = \frac{2P_{\rm ASE}}{h\nu B(G-1)} \tag{12}$$

where $P_{\rm ASE}$ is the power of the amplified spontaneous emission, h is Planck's constant, ν is frequency of the input signal, B is the bandwidth used for the measurement and G is the gain. By using (5), (6), and (8), we can use the measured $n_{\rm sp}$ values of each amplifier to calculate the output means and output variances. We find the $n_{\rm sp}$ values of the different amplifiers in our system to be 1.58, 2.01, 2.04, 2.45, and 2.56.

As a test of this model, we compare the numerical model of the EDFA's with the analytic equations for cascaded amplifiers and find good agreement as, shown in Fig. 10. For this test, we

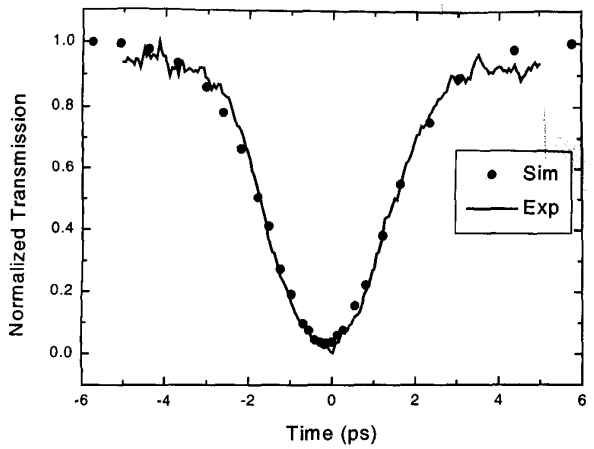

Fig. 11. Timing window of Gate 1. The solid line shows the experimentally measured timing window for the first gate, and the dots represent the simulation timing window used in the model.

assume an ideal input source with Poisson distribution for the noise parameter and a n_{sp} value of 2 for each of the amplifiers and a lumped loss element between each amplifiers. The loss element introduces loss to balance the gain of the amplifier in each segment.

The other sources of noise are the timing jitter and ISI. The timing jitter is modeled as a uniform random variable with a 0.5 ps variance centered at the center of the eye diagram. This value is calculated using the cross-correlation and autocorrelations for the two synchronized lasers [1]. This timing jitter between the incoming packet and the locally generated clock pulses translates into an amplitude jitter out of the first gate for the header processor. The degree of this transfer of jitter is determined by the timing window of the first gate, where a flatter timing window can reduce most of the jitter. The timing window for our device is shown in Fig. 11, which shows for a 0.5 ps variance in timing jitter, there could be significant effects on the performance. The other factor, which is the ISI, is included in the propagation portion of the simulation model where any pulse interactions will be reflected within the code. We will look at any pulse-to-pulse interactions by looking at the tail of the pulse for the various patterns.

In addition, the PMT also generates noise because of the gain produced in the detection scheme. Assuming the input signal to the PMT is Gaussian, the SNR at the PMT becomes

$$\text{SNR} = \frac{i^2}{\sigma_g^2 + \sigma_r^2} \tag{13}$$

where the first term in the denominator is the gain noise and the second term is the circuit noise [14]. The numerator is the square of the mean current generated by the incoming signal. After calculation and substitution for the generated currents from the incoming photons and assuming the circuit noise is negligible compared to the gain noise, the SNR of the incoming signal degrades by the factor $(1/F)$, where F is known as the excessive gain noise. This F factor is typically between "1" and "2" for PMT's [14], and we set it to be "2" for our model because we used a high drive voltage for the PMT.

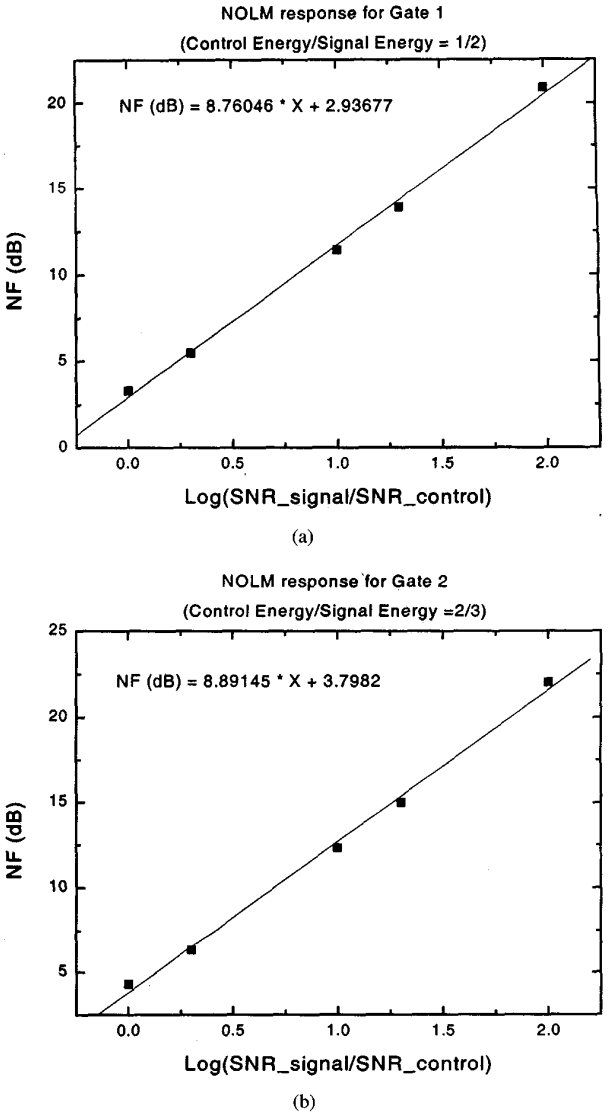

Fig. 12. NF degradation calculated for each of the logic gates. (a) Gate 1 and (b) Gate 2. The numerical data is fitted using a linear fit for each gate with the NF being a function of input energies and input SNR's.

The NOLM will also add some noise to the output signal because the output is an interaction of two or three input signals, which have noise on them. Because there is no real analytic solution for calculating the NF for a NOLM, we study it numerically, and find the approximate equation for the NF as a function of the ratio of the incoming input energies and the ratio of the incoming SNR's. Fig. 12(a) shows the degradation of NF in gate 1 as we change the ratio of incoming SNR's, and Fig. 12(b) shows degradation of NF in gate 2.

We can look at the SNR degradation of the system based upon the NF's of the amplifiers, NOLM's, and PMT. By using the analytic calculations for each of the amplifiers, the calculated NF's for each of the NOLM's as shown in Fig. 12, and with the 3 dB degradation from the PMT, we calculate the overall degradation of the SNR to be 11.7 dB. However, this SNR cannot be directly related to the Q value for this

system because it does not include several key effects. First, there is uneven switching found in the second gate of the header processor due to the fact the unequal pulse widths interact in the loop, which is too short to have a full walk-through. Consequently, when the energies are set to have the best balancing possible (i.e., $1 \oplus 1 = 0$), the individual "1" bits are not at the same level. Second, due to pump leakage from each gate, there is a spread of the "0" level. Third, as mentioned above, the timing jitter will also close the eye diagram due to amplitude jitter. Fourth, pulse quality can also affect the performance by degrading the switching contrasts for each of the gates.

To include all of these additional effects, we numerically model the low-bi-NOLM by the use of the coupled nonlinear Schrödinger equation (NLSE) for birefringent fibers [15] with the addition of noise sources, which were discussed above. These equations include the birefringent walk-off between two orthogonally polarized pulses, group velocity dispersion, self-phase modulation, cross-phase modulation, and the Raman effect. In addition, we include a chirp parameter that is represented in the pulse by

$$u(t) = u_0 \operatorname{sech}\left(\frac{t}{\tau}\right) \exp\left(-\frac{iC_p t^2}{2\tau^2}\right) \tag{14}$$

where C_p is the chirp parameter [16] and u_0 is the amplitude. The chirp on the pulse has a large effect on the pulse evolution within the loop, which could affect both the timing window and output pulse shape. We include the chirp parameter because the EDFL produces slightly chirped pulses.

In the simulation, we convert all the measured values to standard normalized soliton parameters [15]. These parameters are calculated by using the following equations. The soliton period is given by

$$Z_0 = \frac{0.322\pi^2 c\tau^2}{\lambda^2 |D|} \tag{15}$$

where c is the speed of light in free space, τ is the pulse width, λ is the center wavelength, and D is the dispersion. The walk-off length, l_{wo}, defined to be the length required for the peaks of two pulses to separate by one pulse width, is

$$l_{\text{wo}} = \frac{c\tau}{\Delta n} \tag{16}$$

where Δn is the birefringence. The normalized birefringence is given by

$$\delta = \frac{\pi \Delta n \tau}{1.763\lambda^2 |D|}. \tag{17}$$

The fundamental soliton peak power is given by

$$P_c = \frac{\lambda A_{\text{eff}}}{2\pi n_2 Z_c} \tag{18}$$

where A_{eff} is the effective are of the fiber and n_2 is the Kerr coefficient for fiber. Also, Z_c is the characteristic length given by

$$Z_c = \frac{2Z_0}{\pi}. \tag{19}$$

TABLE I
THE PARAMETERS FOR THE TWO LOGIC GATES USED IN SIMULATIONS. THE λ_0 IS 1518 nm FOR BOTH LOGIC GATES. THE INPUT PULSE WIDTH IS 2 ps, AND THE WAVELENGTH IS 1535 nm

	GATE 1	GATE 2
Length of Gate	340 m	260 m
Soliton Period, Z_0	1359 m	1359 m
Walkoff Length, l_{wo}	182 m	167 m
Normalized Birefringence, δ	4.192	4.573
Control Amplitude, u	1.4 (before system)	N/A
Signal Amplitude, v	0.445 (before system)	N/A
Chirp, C_p	0.0-0.44	N/A

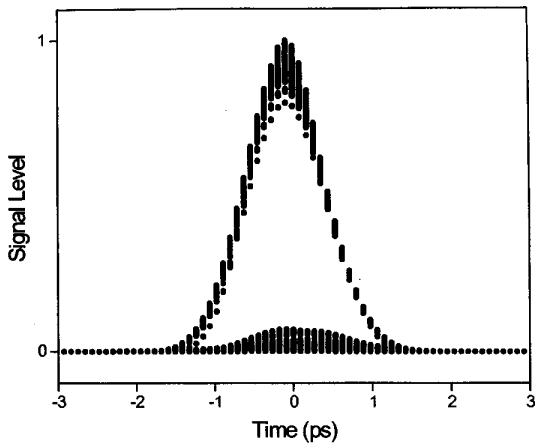

Fig. 13. Simulation result for eye diagram of header processor (simulated pulse). It is an overlay of all the different possible combinations of the 2-bit incoming header and the two possible values of "0" or "1" for the local bit.

From these the control and signal amplitudes are calculated by

$$u = \sqrt{\frac{P_u}{P_c}}$$
$$v = \sqrt{\frac{P_v}{P_c}} \tag{20}$$

where P_u and P_v are the peak powers of the control and signal pulses, respectively. The normalized parameters that are used in the simulations are shown in Table I.

Using the above simulation model with the addition of noise as outlined above, we find the eye diagram for the overall header processor. The eye diagram is shown in Fig. 13. The Q value for this eye is 7.7 and the corresponding calculated BER is 6.8×10^{-15}. The discrepancy from the experimentally measured Q value of 7.1 is probably due to thermal drifts during the time scale of the measurement process, which can change the power levels or polarization states. Also, the varying nonuniformity of the encoders also adds an additional variance that is not included in the model. This nonuniformity cannot be modeled with any steady random distribution because this nonuniformity changes from day to day as well as during the measurement process due to thermal drifts in the fiber and pulse interactions within the encoders. Consequently,

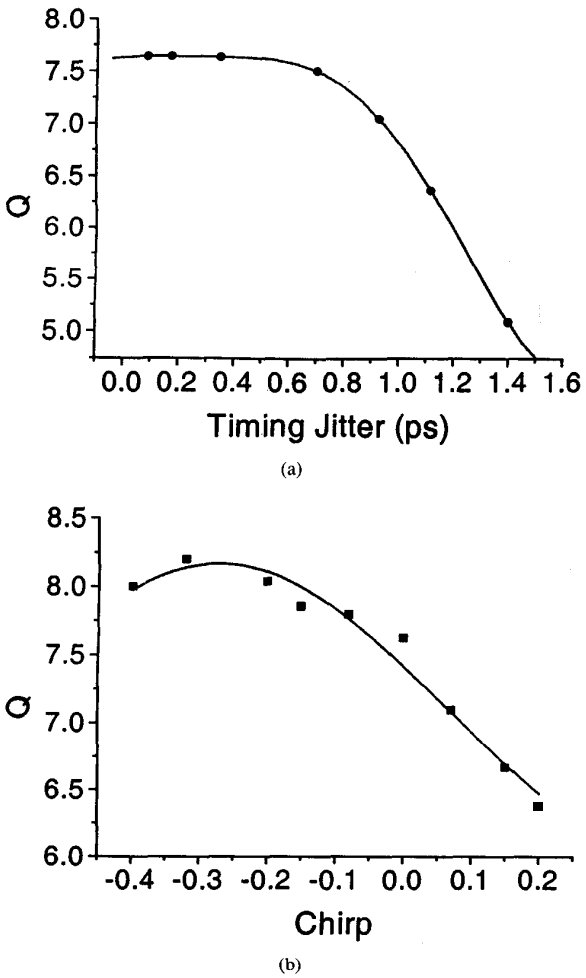

Fig. 14. Degradation of the Q value with (a) increasing timing jitter (b) chirp in local laser. By changing the timing jitter between two synchronous lasers and the chirp in the local laser, a Q value of 8.2 is achievable.

the difference between the simulation and experiment is not unexpected.

We also look at the individual contributions of the various sources of noise. By changing the timing jitter value, local laser chirp and switching energies, we calculate the Q value. We find that the Q value matches the experimental results for jitter values less than 0.6 ps, which is approximately equal to the experimental value of 0.5 ps. Fig. 14(a) shows the change in Q value for different timing jitter values. Since we are using many different types of fibers that may chirp pulses, we simulate the effect of the initial chirp in our local laser. We find that the Q value goes up to 8.2 for negative chirp and gradually decreases as we go to the positive chirp as shown in Fig. 14(b). This indicates that better gate performance may be achieved by adding some chirp to the two input arms.

Using the simulations, we also try to look at pattern dependent effects. We cannot split out this effect from the code. However, by looking at the tails of the pulses for any pulse-to-pulse interaction, we find that there are insignificant differences from the various input patterns with a change of 4% on the performance. Considering the statistical nature of the experiment, this indicates that the ISI from bit-to-bit interaction is negligible. In addition, the energy at the tail is 1.4% of the pump leakage energy. Therefore, the pump leakage dominates any pattern dependent effects on the switching performance. Because of the relatively short length of the header processor (less than 1 km), any ISI effects from pulse-to-pulse interactions should be negligible.

VII. Discussion

Although the simulation results agree with the experimental results, there are some limitations for the sampling technique that must be discussed. First, while the eye diagram is measured experimentally, because of the lack of long, random bit patterns, any long-pattern ISI information cannot be extracted with the technique. However, because the header processor only looks at the packet headers of incoming packets and not at long streams of bits, the long random pattern ISI is not significant. By looking at the different possible patterns as described above, the relevant ISI degradation should be represented. In addition, we find that the most significant cause of degradation is the pump leakage from the wrapped fibers. The second limitation is that the BER values are calculated statistically from the eye diagram assuming a Gaussian noise distribution. Depending on the actual noise distribution, this may give an inaccurate value for the BER. However, the Gaussian assumption generally underestimates the performance because the major contribution of noise is from the amplifiers, which have an exponential noise distribution [17]. Finally, because the BER measurement is a statistical measurement, there is an error bar (confidence interval) associated with the value. This error bar is related to the number of data points (or bits) taken in the sample. For example, for the 1200 points of Fig. 7, the error of the Q value is $\pm 5\%$, and as shown in Fig. 8, the accuracy of the method can be improved by using more points (or bits) without changing the statistical value.

The other limitations are regarding the speed of the measurement technique since the PMT's 10 ns rise and decay time is slower than the bit-to-bit separation or even the packet-to-packet separation. Because we are using a cross-correlator, the signal only appears from the PMT when a reference pulse is present. Consequently, even though the packet repetition rate may be high, as long as the reference pulse used for the performance measurement has a slower repetition rate (larger than 10 ns pulse-to-pulse separation for this PMT), there is no averaging of more than one pulse per sample points. Therefore, the resolution can be set by the pulse width used for the reference pulse. However, the flip side is that because the reference pulse repetition rate can be much slower than the packet rate in a 100 Gb/s system, not all of the packets are used for the eye diagram. The result is that even if we can run the process every 10 ns and assuming 1 ns long packets, we would get 1 out of every 10 packets to be processed in the test. Since the method is a statistical one, performing the statistics on every 10th packet or every packet should be the same. Nevertheless, by using a faster detector (with

40 GHz commercially available) and a faster digital scope (with 50 GHz bandwidth commercially available) to speed up the process, the method can potentially do the statistics using all of the packets. In our experiment, the communication rate between the scope and the computer could be another speed limitation and this limitation can be fixed by storing the eye data on the scope during experiment and downloading and the processing the data after the experiment. The accuracy of the statistical method could be increased by using a fast programmable encoding scheme to change the header of the packet.

VIII. Conclusion

In summary, we have demonstrated and analyzed all-optical serial packet processing for 100 Gb/s words in the off-ramp part of a TDM network access node. The demonstration consists of integrating the various components and looking at the device performance of the off-ramp. The header processor, consisting of two cascaded low-bi NOLM's, has switching energies of 10 pJ/pulse and switching contrast of 10 : 1. The demultiplexer has a switching energy of less than 1 pJ/pulse and switching contrast of 10 : 1. The packet is routed with a contrast ratio of 17 dB.

We test the system performance of the all-optical header processor driven by two synchronized fiber lasers by measuring the eye diagram. We use a sampling technique to obtain an eye diagram and statistical methods to calculate the Q value and the corresponding BER. We measure an eye diagram with a Q value of 7.1 with a $\pm 5\%$ error for 100 Gb/s word packets, which corresponds to a statistically calculated BER value of 8.8×10^{-12}. Finally, we compare the experimental results with simulation models and find good agreement. The simulations calculate a Q value of 7.7, which corresponds to a BER of 6.8×10^{-15}. We also test the degradation of the Q parameter as a result of timing jitter and chirp, and find that the system performance can be improved by adjusting the initial pulse quality and reducing the timing jitter between the two synchronized lasers. This demonstration is used to study the integration issues for combining several different optical components for all-optical packet processing. In addition, the system performance measurement shows that such integration is possible with acceptable performance.

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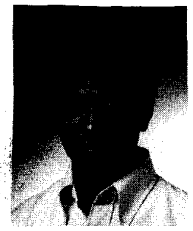

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